REMARKS

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

It is noted that claims 5-6, 13, 17 and 21 are objected to but would be allowable if rewritten in independent form.

Claims 1-4, 7-8 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmuro, *et al.* (U.S. Publication Number 2006/0017677). Claims 9-12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmuro, *et al.* in view of Younis, *et al.* (U.S. Patent Number 6,292,122). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-13, a response time accelerator for driving a liquid crystal display (LCD) includes a frame memory unit that updates and stores one or more frames of previous data and an acceleration unit that performs interpolations on a decoded mapped panel output value and mapped panel characteristic value according to a flag information and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit.

In the present invention as claimed in claims 14-21, a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit includes performing interpolation on a decoded predetermined mapped panel output value according to flag information and generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit. The method further includes performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit.

Ohmuro, *et al.* discloses that a compensation circuit 52 comprises primary and secondary frame memories 53, 54 for alternatively storing a target drive signal S12 of each of respective liquid crystal pixels of an MVA type liquid crystal panel 1 in each

frame period. A display status change pixel detection circuit 55 compares data of the primary frame memory 53 with data of the secondary frame memory 54. The target drive signal S12 in correspondence with the transmittance of the pixels is output from a drive control part 50 and is alternately stored in the primary and secondary frame memories 53, 54 in each frame period. In this case, for example, when the first transmittance of a certain pixel is stored in the primary frame memory 53 in the first frame period and the second transmittance of the pixel is stored in the secondary frame memory 54 in the second frame period. The display status change pixel detection circuit 55 outputs a compensation voltage signal S14 to a drive voltage adjustment circuit 57. The drive voltage adjustment circuit 57 adds the compensation voltage signal S14 to the target drive signal S12 and supplies it to a source driver part 59 and the drive signal S13.

Ohmuro, *et al.* fails to teach or suggest a response time accelerator for driving a liquid crystal display (LCD) that includes a frame memory unit that updates and stores one or more frames of previous data, as claimed in claims 1-13. Instead, in Ohmuro, *et al.*, the target drive signal S12 represents the transmittance of a certain pixel. For example, the first transmittance of a certain pixel is stored in the primary frame memory 53 in the first frame period and the second transmittance of the pixel is stored in the secondary frame memory 54 in the second frame period. Therefore, transmittance of a pixel is stored in frame memories 53 and 54, not previous data, as the applicants claim. Further, Ohmuro, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13. Instead, in Ohmuro, *et al.* the primary and secondary frame memories 53 and 54 both receive the target drive signal S12 from the drive control part 50 and the drive voltage adjustment circuit outputs the drive signal S13 only to the source driver part 59. Therefore, in Ohmuro, *et al.*, previous data of a next frame are not output from the display status change pixel detection circuit 55 or the drive voltage adjustment circuit 57 to either of the primary frame memory 53 or the secondary frame memory as claimed. In addition, target drive signal S12 is not generated by interpolation, as the applicants claim.

In addition, Ohmuro, *et al.* fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21. Instead, in Ohmuro, *et al.* the primary and secondary frame memories 53 and 54 both receive the target drive signal S12 from the drive control part 50 and the drive voltage adjustment circuit outputs the drive signal S13 only to the source driver part 59. Therefore, in Ohmuro, *et al.*, previous data of a next frame are not output from the display status change pixel detection circuit 55 or the drive voltage adjustment circuit 57 to either of the primary frame memory 53 or the secondary frame memory as claimed.

Hence, Ohmuro, *et al.* fails to teach or suggests elements of the present invention set forth in claims 1-13 and 14-21. Specifically, Ohmuro, *et al.* fails to teach or suggest a response time accelerator for driving a liquid crystal display (LCD) that includes a frame memory unit that updates and stores one or more frames of previous data and an acceleration unit that performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13, and a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-4, 7-8 and 14-16 under 35 U.S.C. § 103(a) based on Ohmuro, *et al.* is respectfully requested.

Younis, *et al.* is cited in the Office Action as teaching predetermined mapped panel output values and predetermined mapped panel characteristics values correspond

one-to-one to gray level values determined by MSB bits of the current data and previous data.

Like Ohmuro, *et al.*, Younis, *et al.* fails to teach or suggest a response time accelerator for driving a liquid crystal display (LCD) that includes a frame memory unit that updates and stores one or more frames of previous data and an acceleration unit that performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13. Younis, *et al.* further fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21.

Hence, neither of Ohmuro, *et al.*, as discussed above, and Younis, *et al.* teaches or suggests specific elements of the present invention set forth in claims 1-13 and 14-21. Specifically, neither reference teaches or suggests a response time accelerator for driving a liquid crystal display (LCD) that includes a frame memory unit that updates and stores one or more frames of previous data and an acceleration unit that performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13, and a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in the claims 1-13 and 14-21.

Therefore, it is believed that the claims 1-13 and 14-21 are allowable over the cited references, and reconsideration of the rejections of claims 9-12 and 18-20 under 35 U.S.C. § 103(a) based on Ohmuro, *et al.* and Younis, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 12/6/06

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0457\amendmenta.doc

Steven M. Mills
Registration Number 36,610
Attorney for Applicants